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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,316	04/10/2002	Joseph A. Iadanza	BUR920010123	6885

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,316	IADANZA, JOSEPH A.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-12,15 and 18* is/are rejected.

7)☒ Claim(s) *5-7,13,14,16,17,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/1/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 9 and 11 of remarks, filed 11/22/2005, with respect to the rejection(s) of claim(s) 1, 8, 15, and 18 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejections has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Schneider (U.S. 6,201,829), Ramammurthy (U.S. 5,787,114), Drost et. al., (U.S. 6,076,175) and Variyam (U.S. 6,661,266).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (U.S. 6,201,829) in view of Dorst et. al.,(U.S. 6,076,175) and Variyam (U.S. 6,661,266).

With respect to claim 1, Schneider discloses: a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network (Fig. 5, transmitter side of transceiver, elements 50, 52, 54, 40, column 7, lines 37-39, 41-57) and for continuously generating an output signal corresponding to the data signal; a receiver for continuously

receiving the output signal from the transmitter, and for reconstructing the network data signal within the predetermined time window (Fig. 5, receiver side of transceiver, column 7, lines 58-67, column 8, lines 1-4); and a built-in-self-test (BIST) device for generating the network data signal and the control signal (Fig. 5, combination of elements 61, 62, column 8, lines 32-47, , wherein the BIST device detects erroneous performance by the transceiver based on the reconstructed network data signal (column 8, lines 48-67). Schneider does not expressly teach: the transmitter receiving a control signal for impairing characteristics of the network data signal and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window; and the BIST device generating the control signal and for providing a clock signal with a varied offset for jitter testing of the network data signal. In the same field of endeavor, Drost et. al., disclose: a transmitter receiving a control signal for impairing characteristics of the network data signal and for continuously generating an output signal corresponding to the data signal and the control signal during a predetermined time window (Fig. 3 and Fig. 7, column 3, lines 18-33, column 5, lines 54-67, column 6, lines 1-5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the system of Drost et. al., to determine an actual BER of chips (column 7, lines 11-20). In the same field of endeavor, Variyam et. al. disclose: a BIST device generating a clock signal with a varied offset for jitter testing of the network data signal (Fig. 4, column 4, lines 23-55, column 6, lines 43-56, column 7, lines 1-14, Fig. 11, clock signal with varied offset is shown by MUX_OUT). At

the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the BIST device jitter measuring circuit in the BIST analyzer of Drost et. al., to evaluate the jitter of the clock signal extracted by the receiver PLL and the PLL performance.

With respect to claim 2, all of the limitations of claim 2, are analyzed above in claim 1, and Drost et. al., discloses: the control signal includes signals for impairing a phase and an amplitude of the network data signal (column 3, lines 32-34)(the control signal impairs the transmit clock signal and as a result the network data signal causing timing (phase) errors and amplitude (depending on the amount of jitter of the transmit clock, data bits corresponding to "1" or "0" can be missed). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the system of Drost et. al., to determine an actual BER of chips (column 7, lines 11-20).

With respect to claim 3, all of the limitations of claim 3, are analyzed above in claim 1, and Drost et. al., discloses: a jitter control system (Fig. 7, column 3, lines 26-28). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use jitter control system of Drost et. al., in the BIST of Schneider because the jitter control system (part of the BER evaluation system) allows for determination of an actual BER of chips (column 7, lines 11-20).

With respect to claim 4, all of the limitations of claim 4, are analyzed above in claim 3.

4. Claims 8, 15, 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et. al., (U.S. 5,787,114) in view of Dorst et. al.,(U.S. 6,076,175). With respect to claim 8, Ramamurthy et. al., discloses: a transmitter for receiving a network data signal representative of a signal capable of being transmitted over a network (Fig. 3, "Transmitter", column 5, lines 34-36) and a control signal for impairing characteristics of the network data signal, and for continuously generating an output signal corresponding to the data signal during a predetermined time window; a receiver for continuously receiving the output signal from the transmitter (Fig. 3, "Receiver", column 5, lines 26-34), and for reconstructing the network data signal within the predetermined time window (column 5, lines 26-34); and a built-in-self-test (BIST) device for generating the network data signal (column 5, line 35),wherein the BIST device comprises means for detecting erroneous performance by the transceiver based on the reconstructed network data signal (column 5, lines 33-34, column 7, lines 52-54). Ramamurthy et. al., do not disclose: the transmitter receiving a control signal for impairing characteristics of the network data signal, and continuously generating an ouptut signal corresponding to the data signal and the control signal; and varying the pulse width of the network data signal. . In the same field of endeavor, Drost et. al., disclose: a transmitter receiving a control signal for impairing characteristics of the network data signal and for continuously

generating an output signal corresponding to the data signal and the control signal during a predetermined time window (Fig. 3 and Fig. 7, column 3, lines 18-33, column 5, lines 54-67, column 6, lines 1-5). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the system of Drost et. al., in the system of Ramamurthy et. al., to distort the transmitted network data in order to determine an actual BER of chips (Drost et. al., column 7, lines 11-20), (notice also that using the system of Drost et. al., also results in distortion of the pulse width of the transmitted network data).

With respect to claim 9, all of the limitations of claim 9, are analyzed above in claim 8 and Drost et. al., discloses: the control signal includes signals for impairing a phase and an amplitude of the network data signal (column 3, lines 32-34)(the control signal impairs the transmit clock signal and as a result the network data signal causing timing (phase) errors and amplitude (depending on the amount of jitter of the transmit clock, data bits corresponding to "1" or "0" can be missed). At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the system of Drost et. al., to determine an actual BER of chips (column 7, lines 11-20).

With respect to claim 10, all of the limitations of claim 10 are analyzed above in claim 8, and Ramamurthy et. al., disclose: wherein the BIST device comprises means for programming the network data signals (column 5, line 36).

With respect to claim 11, all of the limitations of claim 11 are analyzed above in claim 8, and Ramamurthy et. al., disclose: wherein the transmitter and the receiver are provided on a single integrated circuit, the transceiver further comprising a transfer gate for selectively coupling the output signal from the transmitter to the receiver within the integrated circuit (column 7, lines 22-32)(transfer gate using FER, bipolar, or other semiconductor transfer gate).

With respect to method claim 15, method claim 15 is analyzed similarly to apparatus claim 8.

With respect to claim 18, the program product restates the function of the specific steps of method claim 15, and is rejected similarly.

5. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et. al., (U.S. 5,787,114) and Dorst et. al.,(U.S. 6,076,175), as applied to claim 8, and view of Variyam et. al., (U.S. 6,661,266).

With respect to claim 12, all of the limitations of claim 12, are analyzed in claim 8 and Ramamurthy et. al., disclose: wherein the network data signal includes an embedded clock signal (column 7, lines 49-51) , Ramamurthy et. al., do not expressly teach: the BIST device comprises means for locking onto the embedded clock signal. In the same field of endeavor, Variyam discloses: a BIST device comprises means for locking onto the embedded clock signal (column 3, lines 15-19, and Fig. 4). At the time of the invention, it would have

been obvious to a person of ordinary skill in the art to incorporate the teachings of Variyam et. al., to lock onto a PLL generated clock (the system of Ramamurthy et. al, has a CDR section where a PLL is commonly used for clock extraction) and measure clock jitter (Variyam, column 3, lines 10-13).

Allowable Subject Matter

6. Claims 5-7, 13-14, 16-17, 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JAY PATEL can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/9/2005
SV

JAY K. PATEL
SUPERVISORY PATENT EXAMINER